ABSTRACT OF THE DISCLOSURE

A method of forming a bit line contact hole. After transistors are formed on a substrate, a polysilicon layer conformally covers the transistors and the substrate. The polysilicon layer is defined to form an inner landing pad connecting with a doped region. A passivation layer is formed on the inner landing pad, the transistor and the substrate. An insulating layer with a flat surface is then formed on the passivation layer. A contact opening is formed in the insulating layer and the passivation layer to expose the inner landing pad. M0 etching forms a recess of interconnecting landing pad pattern in the upper portion of the contact opening. M0 deposition is then performed. The formed bit line contact structure comprises a bottom layer of a polysilicon inner landing pad, a contact plug and a top layer of an interconnected landing pad.